SY21252

High Efficiency, 100V Input, 2A Asynchronous Step Down Regulator

General Description

The SY21252 develops a high efficiency, current mode adaptive constant off time controlled, asynchronous step-down DC/DC converter capable of delivering 2A output current. The SY21252 operates over a wide input voltage range from 4.5V to 100V and integrates main switch with very low $R_{DS(ON)}$ to minimize the conduction loss. The switching frequency is adjustable from 100kHz to 1MHz using an external resistor. And the device features cycle-by-cycle peak current limitation.

Ordering Information

SY21252 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY21252FCC	SO8E	--

Features

- Low $R_{DS(ON)}$ for Internal N-channel Power FET(TOP):175mΩ
- 4.5-100V Input Voltage Range
- 2A Output Current Capability
- Adjustable Switching Frequency Range: 100kHz to1MHz
- Internal Soft-start Limits the Inrush Current
- Hic-cup Mode Output Short Circuit Protection
- EN ON/OFF Control with Accurate Threshold
- Cycle-by-cycle Peak Current Limit
- 0.8V± 1% Reference Voltage Accuracy
- Compact Package: SO8E

Applications

- Non-isolated Telecommunication Buck Regulator
- Secondary High Voltage Post Regulator
- Automotive Systems
- Electric Bicycle

Typical Applications

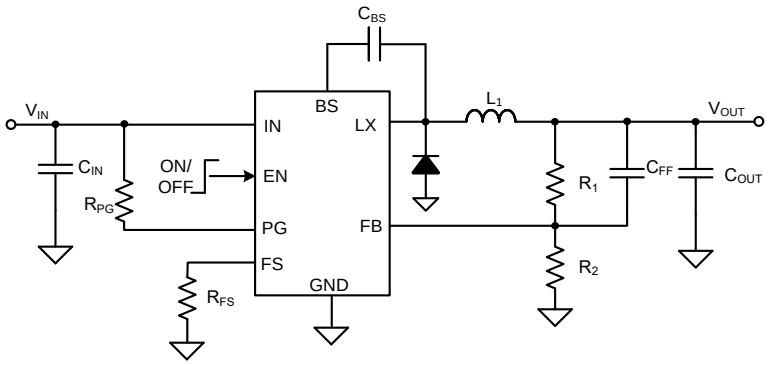


Figure1. Schematic Diagram

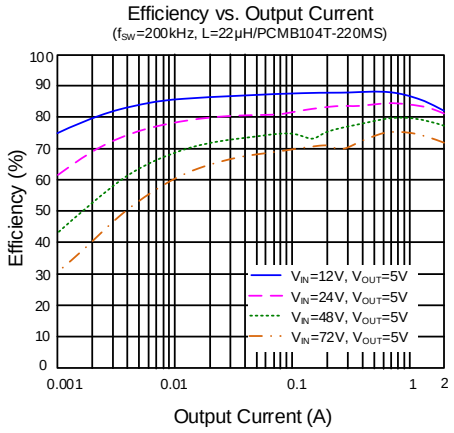
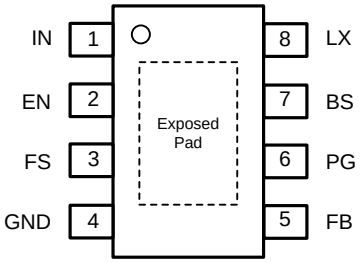


Figure2. Efficiency vs. Output Current

Pinout (top view)



(SO8E)

Top Mark: BXB***xyz*** **(**Device code: BXB; ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
IN	1	Input pin. Decouple this pin to the GND pin with at least a 1μF ceramic capacitor.
EN	2	Enable control. Pulled high to turn on. Do not leave it floating.
FS	3	Frequency programming pin. Connect a resistor to ground to program a switching frequency between 100kHz to 1MHz. The switching frequency equals to: $fsw(kHz)=10^5/R_{FS}(k\Omega)$
GND	4	Ground pin
FB	5	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.8\times(1+R_1/R_2)$.
PG	6	Power good Indicator. Open-drain output when the output voltage is within 90% to120% of the regulation point.
BS	7	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin.
LX	8	Inductor pin. Connect this pin to the switching node of the inductor.
Exposed Pad	/	Exposed pad must be connected to the GND pin. Connect to system ground plane on application board for optimal thermal performance.

Block Diagram

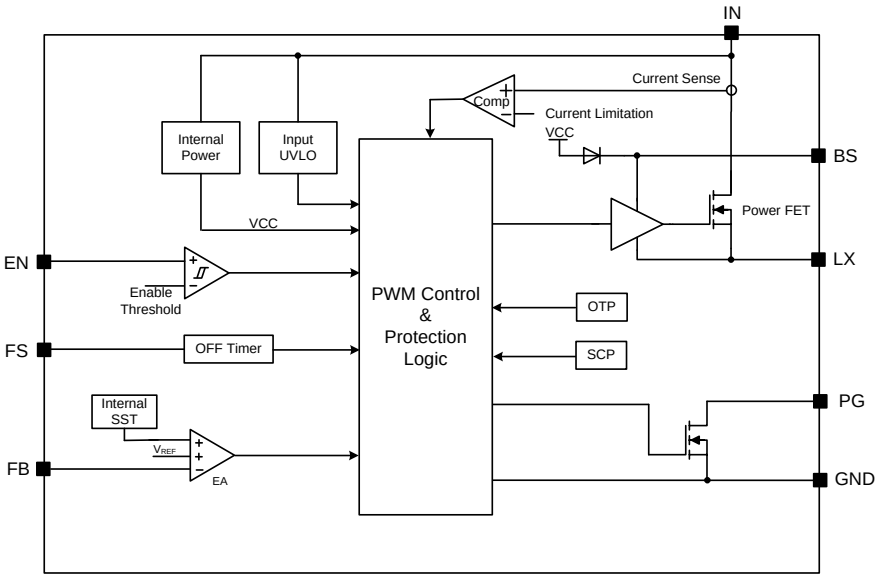


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 100V
BS-LX Voltage ---------- -0.3V to 6V
EN, FS, FB, PG, LX Voltage ---------- -0.3V to V_{IN} + 0.3V
Power Dissipation, P_D @ T_A = 25°C, SO8E ----------2.38W
Package Thermal Resistance (Note 2)
θ_{JA} ----------42°C/W
θ_{JC} ----------4°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX voltage in 10 ns duration ---------- V_{IN} + 3V to GND-5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4.5V to 100V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} =48V, V_{OUT} = 5V, L =10μH, C_{OUT} = 22μF, T_A = 25°C, I_{OUT} =1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		100	V
Input UVLO Threshold	V_{UVLO}		3.9	4.2	4.5	V
Input UVLO Hysteresis	V_{HYS}			0.3		V
Quiescent Current	I_Q	V_{FB}=V_{REF}×105%		100	130	μA
Shutdown Current	I_{SHDN}	V_{EN}=0V	2	8	16	μA
Feedback Reference Voltage	V_{REF}		792	800	808	mV
FB Input Current	I_{FB}	V_{FB}=3.3V	-50		50	nA
Top FET R_{ON}	$R_{DS(ON)}$			175		mΩ
EN Rising Threshold	$V_{EN,R}$		1	1.1	1.2	V
EN Falling Threshold	$V_{EN,F}$		0.8	0.9	1	V
EN Leakage Current	I_{EN}		-1		1	μA
Min ON Time (Note4)	$t_{ON,MIN}$			180		ns
Min OFF Time (Note4)	$t_{OFF,MIN}$			280		ns
Soft-start Time	t_{SS}			2		ms
Switching Frequency Program Range	$f_{SW,RNG}$	R_{FS}=100k~1M	100		1000	kHz
Switching Frequency Setting Accuracy	f_{SW}	R_{FS}=200k	400	500	600	kHz
Power Good Threshold	V_{PG}	V_{FB} falling, PG from high to low		90		%V_{REF}
		V_{FB} rising, PG from low to high		92		%V_{REF}
		V_{FB} rising, PG from high to low		120		%V_{REF}
		V_{FB} falling, PG from low to high		115		%V_{REF}
Power Good Delay (Note4)	t_{PG_F}	High to low		20		μs
	t_{PG_R}	Low to high		200		μs
Power Good Output Low	$V_{PG,L}$	I_{PG}=2mA			0.3	V
PG High Leakage Current					1	μA
Top FET Current Limit	$I_{LMT,RNG}$		3			A
Output Under Voltage Protection Threshold	V_{UVP}		45	50	55	%V_{REF}
Output UVP Delay (Note4)	$t_{UVP,DLY}$			10		μs
UVP Hiccup ON Time	$t_{UVP,ON}$			2		ms
UVP Hiccup OFF Time	$t_{UVP,OFF}$			16		ms
Thermal Shutdown Temperature (Note4)	T_{SD}			150		˚C
Thermal Shutdown Hysteresis (Note4)	T_{HYS}			15		˚C

Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a two-layer Silergy demo board.

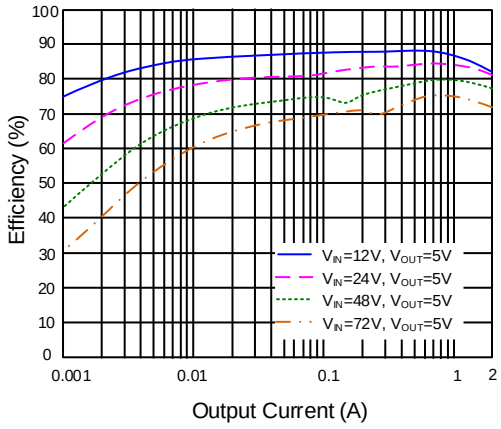
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Based on simulation result.

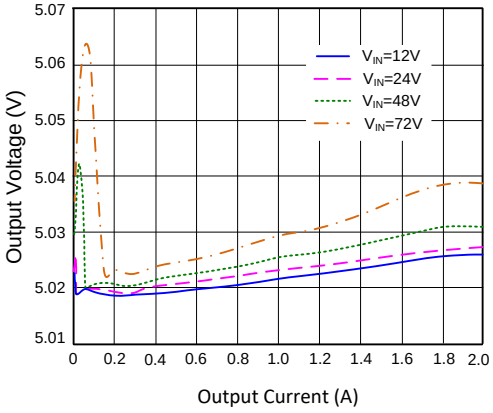
Typical Performance Characteristics

Efficiency vs. Output Current

(f_{SW}=200kHz, L=22μH/PCMB104T-220MS)

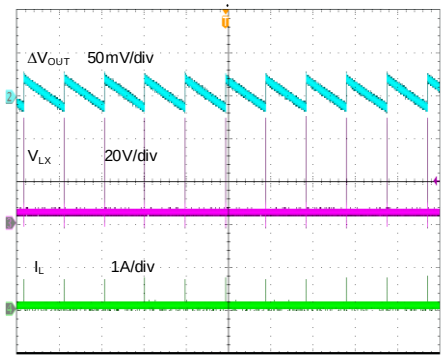


Load Regulation



Output Ripple

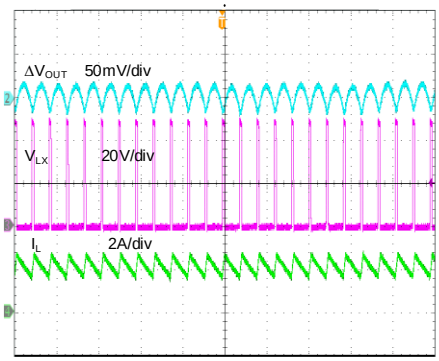
(V_{IN}=48V, V_{OUT}=5V, I_{OUT}=0A)



Time (20ms/div)

Output Ripple

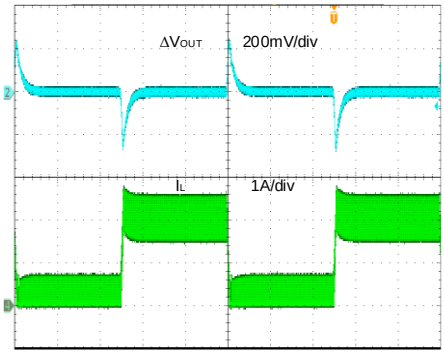
(V_{IN}=48V, V_{OUT}=5V, I_{OUT}=2A)



Time (10μs/div)

Load Transient

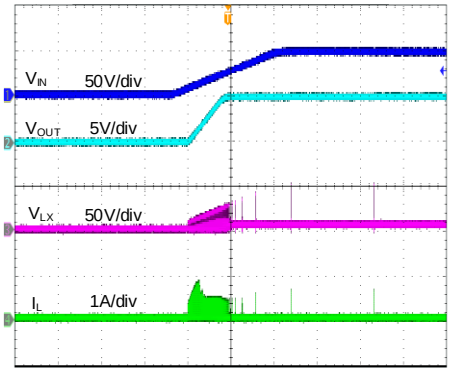
(V_{IN}=48V, V_{OUT}=5V, I_{OUT}=0.2~2A)



Time (400μs/div)

Startup from V_{IN}

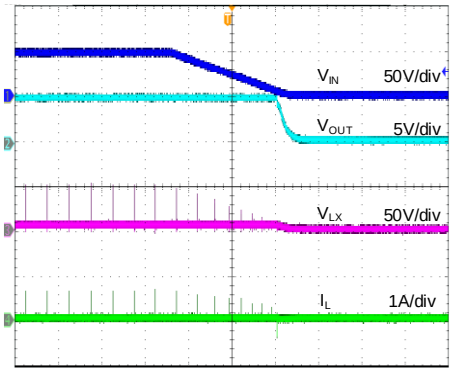
(V_{IN}=48V, V_{OUT}=5V, I_{OUT}=0A)



Time (2ms/div)

Shutdown from V_{IN}

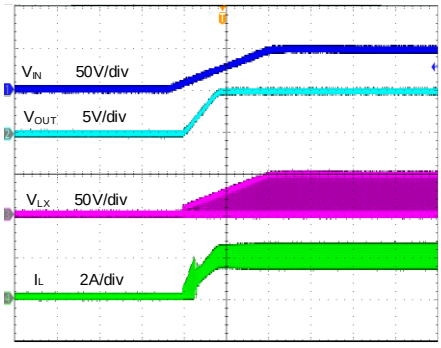
(V_{IN}=48V, V_{OUT}=5V, I_{OUT}=0A)



Time (40ms/div)

Startup from V_{IN}

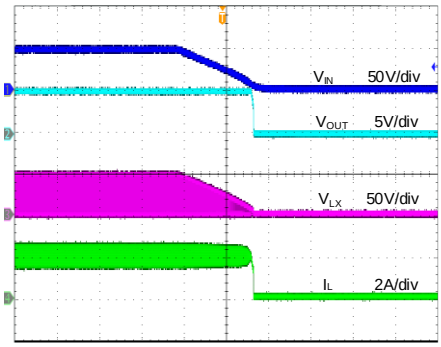
(V_{IN}=48V, V_{OUT}=5V, I_{OUT}=2A)



Time (2ms/div)

Shutdown from V_{IN}

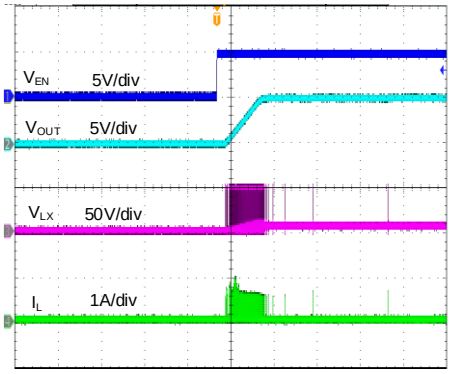
(V_{IN}=48V, V_{OUT}=5V, I_{OUT}=2A)



Time (40ms/div)

Startup from EN

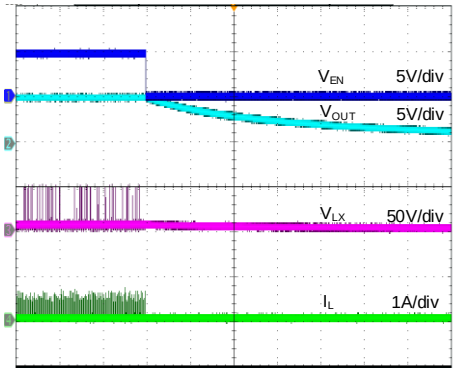
(V_{IN}=48V, V_{OUT}=5V, I_{OUT}=0A)



Time (2ms/div)

Shutdown from EN

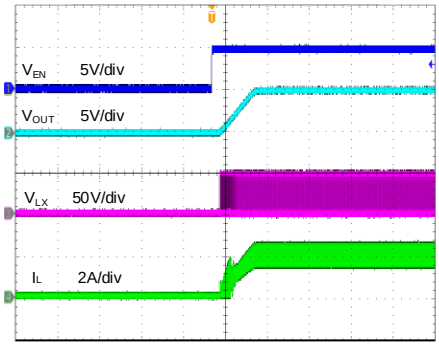
(V_{IN}=48V, V_{OUT}=5V, I_{OUT}=0A)



Time (1s/div)

Startup from EN

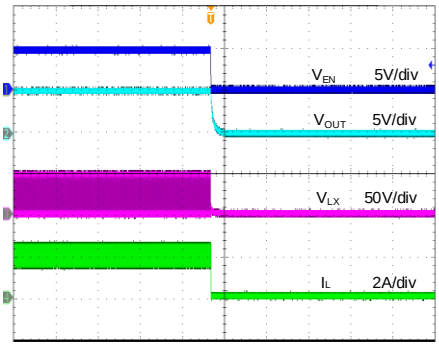
(V_{IN}=48V, V_{OUT}=5V, I_{OUT}=2A)



Time (2ms/div)

Shutdown from EN

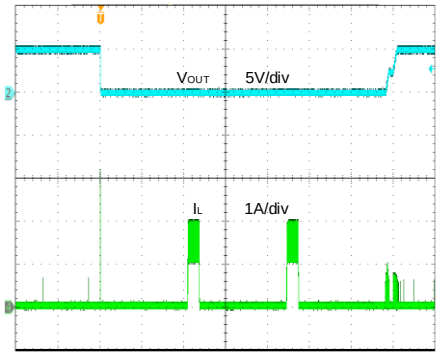
(V_{IN}=48V, V_{OUT}=5V, I_{OUT}=2A)



Time (2ms/div)

Short Circuit Protection

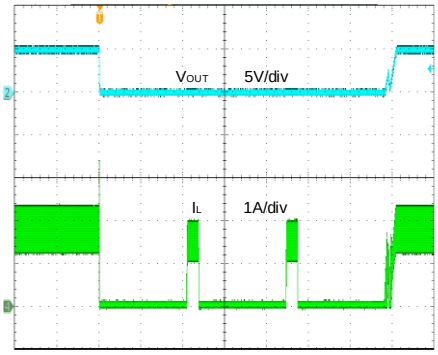
(V_{IN}=48V, V_{OUT}=5V, I_{OUT}=0A~short)



Time (10ms/div)

Short Circuit Protection

(V_{IN}=48V, V_{OUT}=5V, I_{OUT}=2A~short)



Time (10ms/div)

Operation Description

The SY21252 develops a high efficiency, current mode adaptive constant off time controlled, asynchronous step-down DC/DC converter capable of delivering 2A output current. The SY21252 operates over a wide input voltage range from 4.5V to 100V and integrates main switch with very low $R_{DS(ON)}$ to minimize the conduction loss. The switching frequency is adjustable from 100kHz to 1MHz using an external resistor. And the device features cycle-by-cycle peak current limitation.

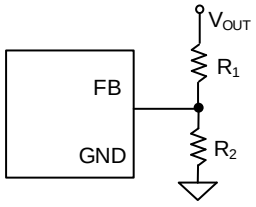
Applications Information

Because of the high integration in the SY21252, the application circuit based on this IC is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, the output inductor L_1 and the feedback resistors (R_1 and R_2) need to be selected for the target applications.

Feedback Resistor Dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If V_{OUT} is 5V, R_1=105kΩ is chosen, then using the following equation, R_2 can be calculated to be 20kΩ:

$$R_2 = \frac{V_{FB}}{V_{OUT} - V_{FB}} R_1$$, V_{FB} is typical 0.8V.



Input Capacitor C_{IN}:

The ripple current through the input capacitor is calculated as:

$$I_{CIN,\,RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

To minimize the potential noise problem, a typical X5R or better grade ceramic capacitor should be placed really close to the IN and the GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and the IN/GND pins. In this case, a 1μF low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor greater than 22μF capacitance.

Output Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where fsw is the switching frequency and the $I_{OUT,MAX}$ is the maximum load current.

The SY21252 regulator is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > I_{OUT,\,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

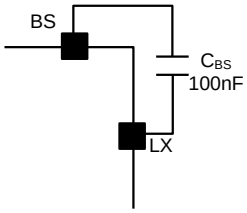
Enable Operation

Pulling the EN pin low (<0.8V) will shut down the device. During the shutdown mode, the SY21252 shutdown current will drop to lower than 16μA. Driving the EN pin high (>1.2V) will turn on the IC again.

It is not recommended to connect EN and IN directly. A resistor in a range of 10kΩ to 1MΩ should be used if EN is pulled high by IN.

External Bootstrap Capacitor

This capacitor provides the gate driver voltage for internal high side MOSFET. A 100nF low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.



Adjustable Switching Frequency:

The FS pin is used for setting the switching frequency of the device by connecting a resistor from the FS pin to GND. The switching frequency of the device is adjustable from 100 kHz to 1MHz.

$fsw(kHz)=10^5/R_{FS}(k\Omega)$

The SY21252 linearly folds back the switching frequency when the FB voltage is within 0~50% of the reference voltage during soft-start and the SCP event. The minimum switching frequency is clamped to 50kHz.

Power Good Indication

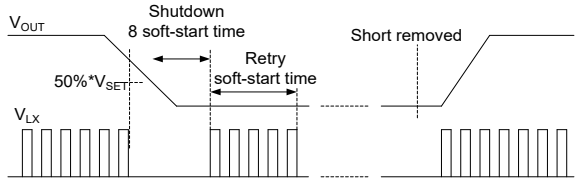
PG is an open-drain output pin. This pin will be pulled to ground if the output voltage is lower than 90% of regulation voltage or higher than 120% of regulation voltage. Otherwise this pin will go to a high impedance state.

Over-current Protection (OCP)

The SY21252 features cycle-by-cycle peak current limit. When the peak current limit is triggered, the device will turn off the high side MOSFET and turn on the low side MOSFET until the next cycle clock is coming.

Short-circuit Protection (SCP)

If V_{OUT} < 50% of the set-point continuously for approximately 10μs, the short-circuit protection mode will be initiated, and the device will shut down for 8 soft-start time. The device will then restart with a complete soft-start cycle. If the short circuit condition remains, another 'hiccup' cycle of shutdown and restart will continue indefinitely.



Over-temperature Protection (OTP)

The device includes over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 15°C the IC will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

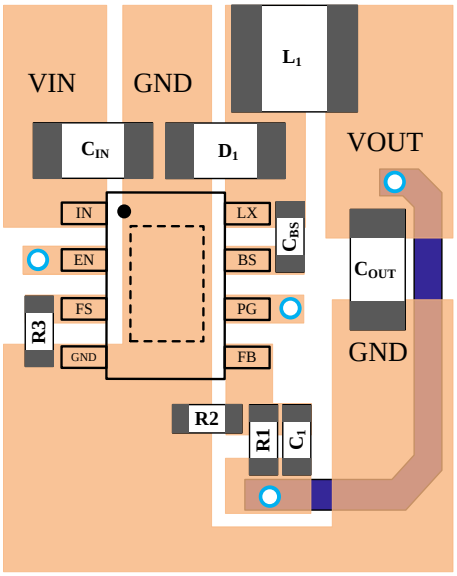
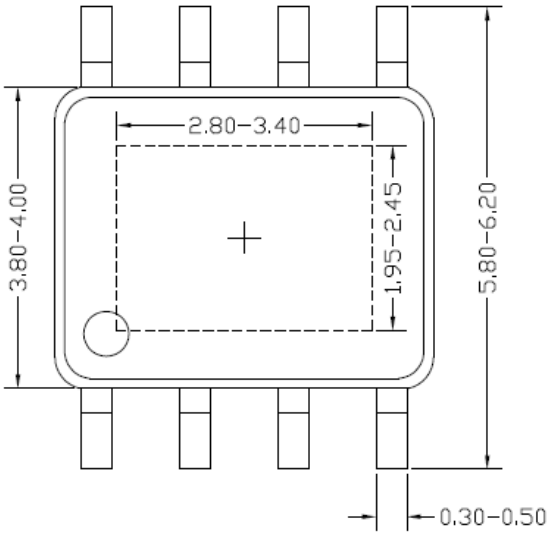
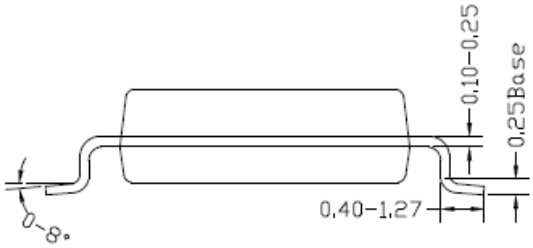


Figure4. PCB Layout Suggestion

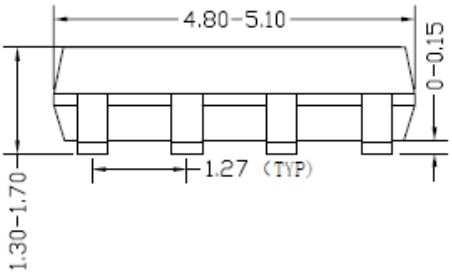
SO8E Package Outline & PCB Layout



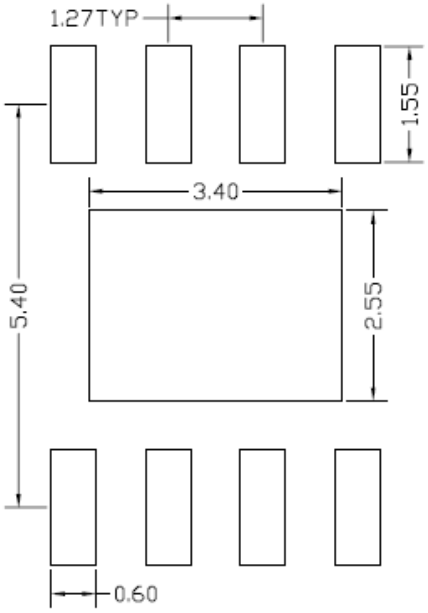
Top view



Side view



Front view



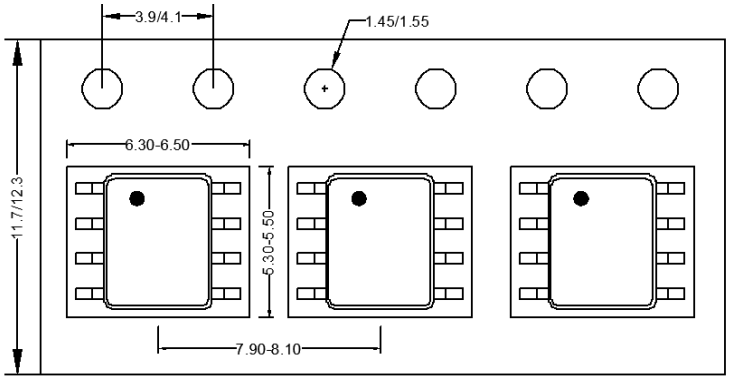
Recommended PCB Layout
(Reference Only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

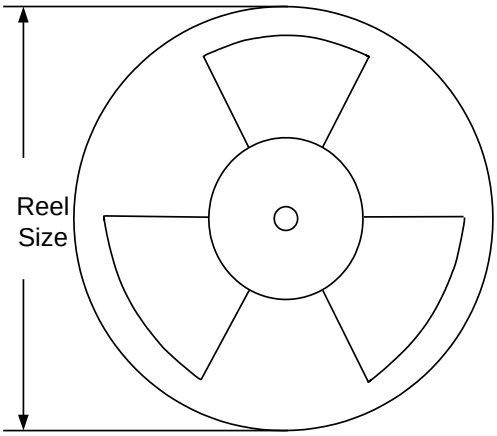
1. Taping orientation

SO8E



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SO8E	12	8	13"	400	400	2500

Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
July 01, 2022	Revision 0.9	Initial Release

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